NEWS ALERT

Analog Bits to Participate in a Customer Test Chip Tapeout on TSMC A14 and Present Papers with Cerebras, Arm and Socionext on Real-Time On-Chip Power Sensing and Delivery at 2026 TSMC Global OIP Ecosystem Events

At TSMC 2026 North America OIP Ecosystem Forum, Analog Bits will showcase new real-time power observability and sensing analog IP in TSMC's N2P process technology and present a paper with Cerebras; Papers planned with partners at global OIP Ecosystem events to highlight smarter power delivery for scalable SoCs targeting data centers, automotive and more.

Sunnyvale, CA, September 21, 2026 – Analog Bits (www.analogbits.com), developer of industry leading low-power mixed-signal IP (intellectual property) solutions for intelligent power and energy management, today announced inclusion of its IP in an upcoming tape out of a customer test chip on TSMC's A14 process. Further, at this week's TSMC 2026 North America Open Innovation Platform® (OIP) Ecosystem Forum, the company will present a paper with Cerebras to highlight on-die power management for scalable SoCs and chiplet architectures. Analog Bits will also present a paper with Socionext at the virtual edition of TSMC 2026 North America OIP Ecosystem Forum and with ARM at multiple TSMC Global OIP Ecosystem events.

Analog Bits has a long history of partnering with TSMC, providing its best-in-class IP in the latest advanced processes. This tradition continues with the test chip on TSMC's A14 process technology, aimed at ensuring that the portfolio of next-generation IP is silicon-proven to enable mutual customers. This is in addition to a whole suite of IP for TSMC's N2P process technology to be demonstrated by Analog Bits at the 2026 OIP Ecosystem Forum. The company will showcase new integrated on-die LDOs with glitch catcher and droop detection, pinless PVT sensors, and low-power PLLs that deliver comprehensive real-time power observability and sensing. Also featured will be the highly accurate remote pinless PVT sensors with a +/-3.5C (untrimmed), and low-power PLLs that feature microwatt-class power levels at 0.5 micro-watt/MHz.

This level of power observability capability in advanced nodes is important to manage the thermal, power efficiency, performance variability and reliability challenges in modern megawatt AI and high-performance computing (HPC) systems using multi-kilowatt SoCs. Transistor speeds going up and voltage levels not scaling down proportionally cause more power density challenges, which is why the ability to leverage advanced process and packaging energy-efficiency techniques along with architectural-level optimizations is vital in order to achieve power targets.

Technical Papers

Analog Bits will present papers with Cerebras, Socionext and Arm at the upcoming TSMC 2026 North America and the Europe OIP Ecosystem Forums.

At the TSMC 2026 North America OIP Ecosystem Forum held on September 23, Analog Bits will present a paper co-authored with Cerebras Systems titled “On-Die Power Management for Scalable SoCs and Chiplet Architectures”. The companies will showcase scalable on-die power management IP solutions that address the growing power delivery challenges of advanced SoCs and chiplet-based systems, improving power integrity, energy efficiency, and reliability for AI and high-performance computing applications.

Building on this, Analog Bits will present a co-authored paper with Socionext entitled “Pinless PLL and PVT Sensor IP for Datacenter and Automotive SoCs in Advanced FinFET Nodes” at the virtual edition of North America OIP Ecosystem Forum. Analog Bits will showcase its patented pinless PLL and PVT sensor IP for leading edge TSMC process nodes, eliminating the need for dedicated analog power supplies to simplify integration, reduce system cost, and improve SoC scalability.

Following the North America event, at the TSMC 2026 Europe OIP Ecosystem Forum on November 24, Analog Bits, co-authored with Arm Ltd., will introduce a paper entitled “Datacenter-Scale CPU Power Management using Integrated Power and Clocking in N3/N2 SoCs”. This paper will focus on an integrated on-die power management solution for TSMC N3P and N2P technologies that enables real-time, core-level power optimization for AI and hyperscale datacenter SoCs.

About Analog Bits

Analog Bits, Inc. is an established supplier of an industry-leading portfolio of mixed-signal IP for intelligent energy and power management, with a reputation for easy and reliable integration into advanced SoCs. Its products include precision clocking macros, power and temperature sensors, LDOs and regulators, and programmable interconnect solutions such as multi-rate SERDES and programmable I/O’s. With billions of IP cores fabricated in customer silicon, from 0.35 micron to 2nm processes, Analog Bits has an outstanding heritage of first-time-working IPs that lower risk. For more information and a detailed product selection guide, visit **www.analogbits.com**.

About Socionext Inc.

Socionext Inc., a leading global System-on-Chip (SoC) supplier, is a pioneer of the 'Solution SoC' business model. This innovative approach encompasses Socionext's 'Entire Design' capabilities and offering of 'Complete Service'. As a trusted silicon partner, Socionext fuels global innovation, providing superior features, performance, and quality that set its customers' products and services apart in diverse domains ranging from automotive and data centers to networking, smart devices, and industrial equipment.

Socionext Inc., based in Yokohama, operates offices across Japan, Asia, the United States, and Europe for development and sales. For more information, visit **https://www.socionext.com/en/**.

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