PRESS RELEASE

Analog Bits Adds New Power and Energy Management IP Blocks Proven on TSMC N2P and N3P Processes at TSMC 2025 OIP Ecosystem Forum

Company will demonstrate newest LDOs, PLLs, and sensors proven on TSMC's latest process technologies at the TSMC 2025 Open Innovation Platform® (OIP) Ecosystem Forum in Silicon Valley

Sunnyvale, CA, September 24th – Analog Bits (www.analogbits.com), developer of industry leading low-power mixed-signal IP (intellectual property) solutions for intelligent power and energy management, has announced its newest LDO, power supply droop detectors, embedded clock LC PLL's on the TSMC N3P process, and clocking, high accuracy PVT and droop detectors on the TSMC N2P process. These will be demonstrated live at the Analog Bits booth during the TSMC 2025 North America Open Innovation Platform® (OIP) Ecosystem Forum in Santa Clara, California. This demonstration will showcase Analog Bits' industry leading portfolio of mixed signal IP in TSMC's advanced 5nm, 3nm, and 2nm processes. Analog Bits will also be presenting a joint presentation with Socionext and Cerebras.

Highlights

- Analog Bits will be presenting demos for:
  - High accuracy PVT sensors, high performance clocks, droop detectors, and more on the TSMC N2P process
  - Programmable LDO, droop detector, high accuracy sensors, low jitter LC PLL and more on the TSMC N3P process
  - Automotive grade pinless high accuracy PVT, pinless PLL, PCIe SERDES on the TSMC N5A process
- Analog Bits will also present the following papers:
  - Joint paper with Socionext titled "Pinless PLL, PVT Sensor and Power Supply Spike Detectors for Datacenter, AI and Automotive Applications"
  - Joint paper with Cerebras titled "On-Die Power Management for SoCs and Chiplet" at the virtual event

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"Analog Bits is pleased to be an early partner qualifying IPs on TSMC's N3P and N2P test-chips enabling a complete intelligent power performance architecture for our customers," said Mahesh Tirupattur, CEO at Analog Bits. "Whether you are designing advanced datacenters, AI/ML applications, or automotive SoC's managing power is no longer an afterthought, it has to be done right at the architectural phase. We have collaborated with TSMC and trailblazed on our IP development with advanced customers to pre-qualify novel power management IP's such as LDO, droop detectors, and high-accuracy sensors along with our sophisticated PLL's for low jitter. We welcome customers and partners to see our latest demos at the Analog Bits booth during this year's TSMC OIP event."

When **September 24, 2025**

Register at:
https://pr.tsmc.com/english/events/tsmc-events

Location **Santa Clara Convention Center, Booth #808**

The company will also be participating in other locations of the TSMC OIP Ecosystem Forum event around the world.

Analog Bits, Inc. is the established supplier of an industry-leading portfolio of mixed-signal IP for intelligent energy and power management, with a reputation for easy and reliable integration into advanced SoCs through all the major foundries. Its products include precision clocking macros, power and temperature sensors including LDO and regulators, programmable interconnect solutions such as multi-rate SERDES and programmable I/O's. With billions of IP cores fabricated in customer silicon, from 0.35 micron to 2nm processes, Analog Bits has an outstanding heritage of first-time-working IP's that lower risk. For more information and a detailed product selection guide, visit www.analogbits.com.

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