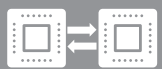


# Low power PCI Gen3/4 SERDES on Samsung SF5A & 7LPP

- ✓ Silicon Proven IP in 7LPP
- ✓ Easy Migration to SF5A
- ✓ Differentiated Low Power PCI Gen4 IP
- ✓ Area and power optimized Gen3 PHY
- ✓ PIPE compliant PHY integrates easily with industry standard controllers



**SERDES**



**Clocking**



**Sensors**

Low Power and  
Optimized for  
Performance PCIe  
SERDES

PLL IP's – Core Power  
Pinless PLL and Ref  
Clock PLL's available  
upon request

Sensor IP's – PVT Sensor  
available and Power  
Supply Sensors available  
upon request