NEWS ALERT

Analog Bits to Demonstrate Low Latency PCIe/CXL Gen 5 on Samsung 8nm at SAFE Forum 2021

Highlights

- Watch our Executive Vice President Mahesh Tirupattur present his paper on PCIe/CXL Gen 5 low latency SERDES in Samsung's advanced process of 8LPP.

Sunnyvale, CA, November 15, 2021 – Analog Bits (www.analogbits.com), the industry's leading provider of low-power mixed-signal IP (Intellectual Property) solutions will be presenting their paper: *"PCIe/CXL SERDES- Gen4/5 Enterprise Class SerDes & Lowest Power Gen3/4 Consumer SERDES in Samsung 28nm to 5nm Processes*" at Samsung Advanced Foundry Ecosystem (SAFE) Forum.

"Analog Bits low latency SERDES is a key differentiator for high-end enterprise SSD's and Re-timer SoC's that are optimizing for performance and throughput," said Mahesh Tirupattur, Executive Vice President at Analog Bits. "And our close collaboration with Samsung gives us the opportunity to help our mutual customers deliver the best possible latency and performance to the end customers in Gen5 and Gen6 in future. We truly appreciate our years of strategic partnership with Samsung."

When **November 17-18, 2021**

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https://www.samsungfoundryevent.com/safe2021

About Analog Bits

Founded in 1995, Analog Bits, Inc. is the leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SoCs. Our products include precision clocking macros, Sensors, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's. With billions of IP cores fabricated in customer silicon, from 0.35-micron to 3nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

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