Analog Bits to Present Papers, Demo of N5 Working Silicon, and Roadmap on IPs for TSMC N4 and N3 Processes

Highlights

- Come and see our demo of these IPs on N5 test-chips 20GHz C2C PLL with very low DJ, 8GHz Low Power PLL for digital SoC application, PVT Sensor, Power Supply Droop Detector, Xtal OSC and Differential Clock Buffers proven on TSMC N5 process
- Paper 1: "Sensing the Unknown: Modern Methods to Designing chips"
- Paper 2: Joint paper with Siemens "Design and Verification of Clocking Macros and Sensors in N5 and N3 Processes Targeting High Performance Compute, Automotive, and IoT Applications."

Sunnyvale, CA, October 26th, 2021 – Analog Bits (<u>www.analogbits.com</u>), the industry's leading provider of low-power mixed-signal IP (Intellectual Property) solutions, will be presenting two technical papers on N5 IPs, demonstrating working Silicon of Foundation IPs Including PLLs, Sensors and IO's Showcases Significant & Broad PPA Benefits of N5 Technology at 2021 TSMC Open Innovation Platform[®] (OIP) Ecosystem Forum. Additionally we will be discussing roadmap for TSMC N5 Automotive grade IPs, N4 and N3 IPs.

"The Analog Foundation IP is a key differentiator for every high-end SoC that is optimizing for performance, power or density," said Mahesh Tirupattur, Executive Vice President at Analog Bits. "Our early and close collaboration with TSMC on advanced nodes allows us to de-risk our mutual customers deliver the highest reliability & quality of IP's. We truly appreciate our years of symbiotic partnership with TSMC."



https://pr.tsmc.com/english/events/tsmc-events



About Analog Bits

Founded in 1995, Analog Bits, Inc. is the leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SoCs. Our products include precision clocking macros, Sensors, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's. With billions of IP cores fabricated in customer silicon, from 0.35micron to 3nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

Contact:

Arthur Rogers <u>arthur@analogbits.com</u>

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Editorial Contact:

Arthur Rogers Analog Bits <u>arthur@analogbits.com</u> (650) 314-0200