## Analog Bits to Demonstrate New High Performance and Ultra-Low Power SERDES IP at TSMC Open Innovation Platform Ecosystem Forum

## Highlights

• Analog Bits will demonstrate two new IP solutions at this TSMC's Open Innovation Platform Ecosystem Forum in Santa Clara, CA.

**Santa Clara, CA, September 13, 2017** – Analog Bits (www.analogbits.com), the industry's leading provider of low-power mixed-signal IP (Intellectual Property) solutions, will be demonstrating two new IP solutions at this TSMC's Open Innovation Platform Ecosystem Forum in Santa Clara, CA.



## Ultra-low power and high performance SERDES IP with support for multiple protocols

- An ultra-low power SERDES IP solution for consumer and automotive applications like PCIe Gen3, SATA3, DP, SGMII, XAUI/RXAUI, etc. with the industry-leading performance/power
- A high performance SERDES IP solution for data-center and enterprise applications like PCIe Gen4, SAS4, 10GKR, and XFI with speeds as high as 25G

These products are in addition to Analog Bits' other leading mixed signal IP products including PVT Sensors and a wide variety of PLLs.







Additionally, Mahesh Tirupattur, Analog Bits' Executive Vice President, will be delivering a presentation entitled **High Reliability IP for Automotive and Datacenter Applications** at 4:00pm in the EDA/IP/Services Track.

## **About Analog Bits**

About Analog Bits: Founded in 1995, Analog Bits, Inc. (www.analogbits.com), is the leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SOCs. Products include precision clocking macros such as PLLs & DLLs, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's, Sensors, as well as specialized memories such as high-speed SRAMs and TCAMs.

With billions of IP cores fabricated in customer silicon, from 0.35-micron to 7-nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

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