NEWS ALERT

Analog Bits to Demonstrate 5nm IP Silicon at TSMC 2021 Online Technology Symposium

Highlights

- **Come and see our demo of these IPs on 5nm test-chips** - 20GHz C2C PLL with very low DJ, 8GHz Low Power PLL for digital SOC application, PVT Sensor, Power Supply Droop Detector, Xtal OSC and Differential Clock Buffers on TSMC's N5 process.

Sunnyvale, CA, May 26, 2021 – Analog Bits (www.analogbits.com), a leading provider of low-power mixed-signal IP (Intellectual Property) solutions, will be demonstrating Silicon of Foundation IPs including PLLs, Sensors and IO's, showcasing significant and broad power, performance and area (PPA) benefits of N5 process at TSMC 2021 Online Technology Symposium.

"The Analog Foundation IP is a key differentiator for every high-end SoC that is optimizing for performance, power or density" said Mahesh Tirupattur, Executive Vice President at Analog Bits. "Our close collaboration with TSMC gives us the opportunity to help our mutual customers deliver the best possible reliability & quality to the end customers. We truly appreciate our years of strategic partnership with TSMC."

When **June 1st, 2021**

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https://www.tsmc.com/static/english/campaign/Symposium2021/index.htm

About Analog Bits

Founded in 1995, Analog Bits, Inc. (www.analogbits.com), is the leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SOCs. Products include precision clocking macros such as PLLs & DLLs, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's as well as specialized Sensors.

With billions of IP cores fabricated in customer silicon, from 0.35-micron to 7-nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

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