Low power PCI Gen3/4 SERDES on Samsung 5LPE & 7LPP

- Silicon Proven IP in 7LPP
- Easy Migration to 5LPE
- Differentiated Low Power PCI Gen4 IP
- Area and power optimized Gen3 PHY
- PIPE compliant PHY integrates easily with industry standard controllers

SERDES

Low Power and Optimized for Performance PCIe SERDES

Clocking

PLL IP's – Core Power Pinless PLL and Ref Clock PLL's available upon request

Sensors

Sensor IP's – PVT Sensor available and Power Supply Sensors available upon request

ANALOG BITS

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