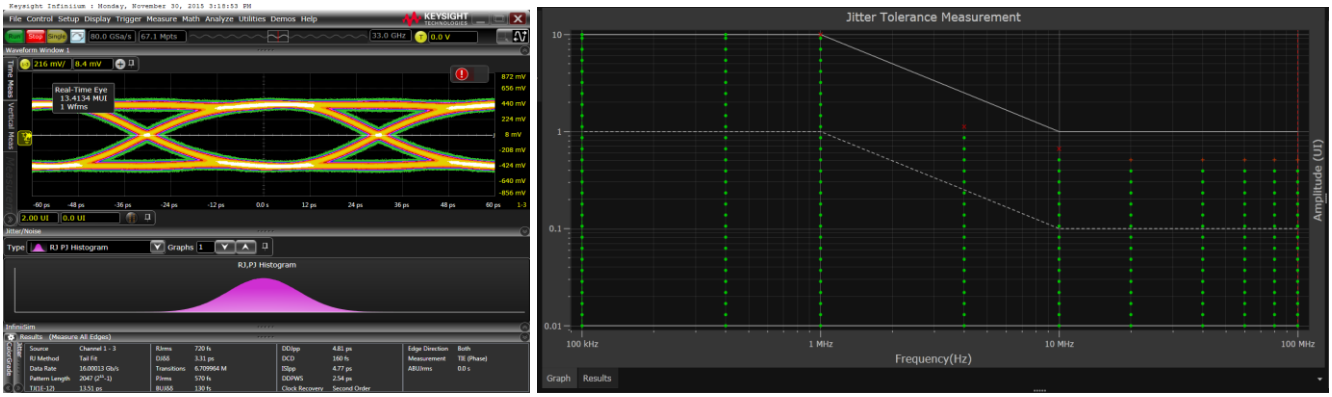
Features

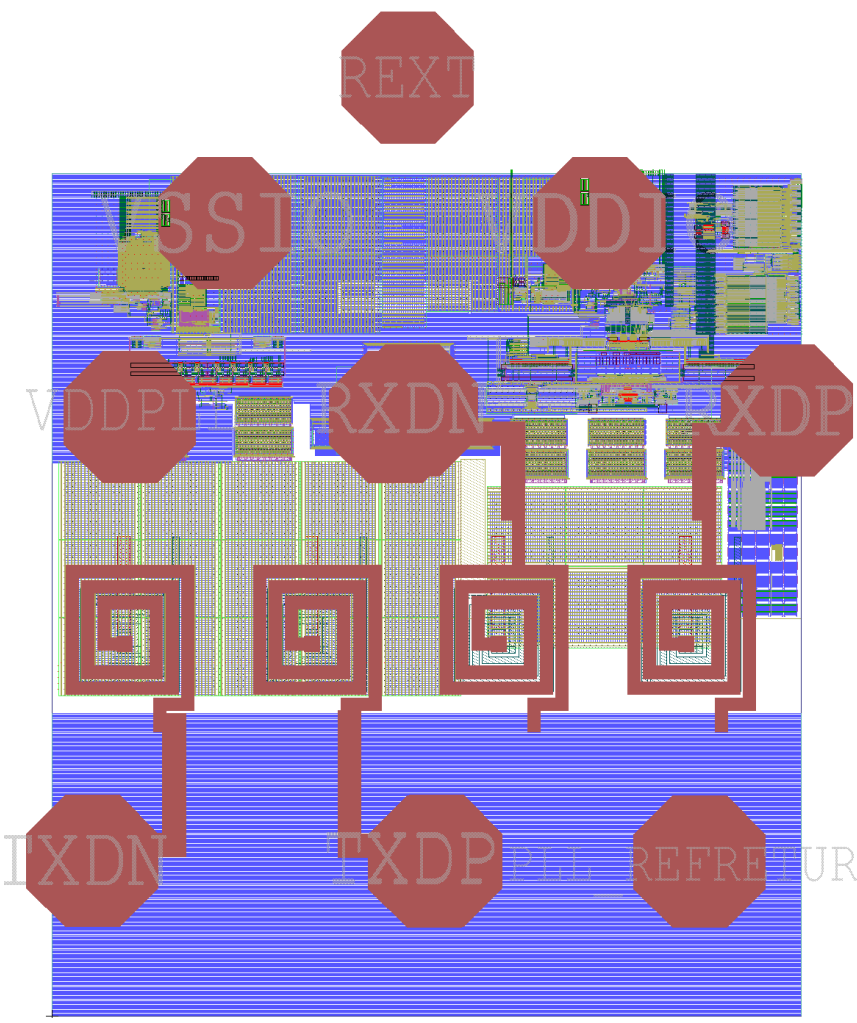
- Industry leading low power PMA macro – 122.9mW per lane at 16Gbps (7.7mW/Gbps) inclusive of Tx and Rx PLLs, termination, bias, etc.
- Support for Ethernet protocols and Automotive Grade 2
- Compact form factor – 0.34 mm^2 active silicon area per lane including ESD
- Minimal latency – 3 UI between parallel transfer and serial transmission
- Single-lane macro scalable to unlimited link width – x1, x2, x4, x8, x16, etc.
- Multi-orientation macros of 4, 8 and 16 lane SERDES are available for most common metal stacks
- Exhibits exceptional input sensitivity, input jitter tolerance and low output jitter
- Finely configurable receiver impedance, CTLE gain and bandwidth, with fully adaptive CTLE and DFE
- Finely configurable driver impedance, amplitude and 3-tap FFE
- Supports multiple low-power modes
- Test support features such as near-end loopback, reverse loopback, PRBS generator+checker, PLL bypass modes, etc.
- Includes PIPE Compliant PCIe PCS with programmable PIPE frequencies, and supporting bifurcation, lane/link powerdown, SRNS, SRIS and L1-substates
- Supports industry standard third-party controllers for PCIe
- Low pin-count and suitable for a variety of flip-chip packages when paired with onchip T-coils
- Metallization scheme and pad/bump structures customizable to specifications

General Description

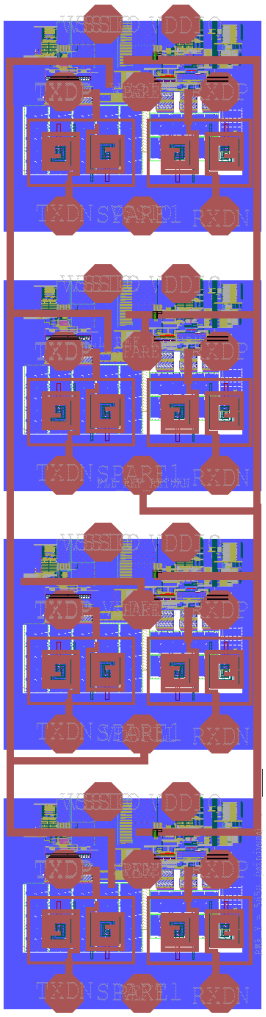
Analog Bits' Programmable SERDES provides a Physical Media Attachment (PMA) Layer and synthesizable Physical Coding Sublayer (PCS). The integrated PHY for PCIe 4.0 operates at 2.5Gbps, 5Gbps, 8Gbps and 16Gbps, and is designed to meet higher performance standards required for enterprise market applications. The PHY additionally features an interface capability that allows integration with other customer-designed serial protocol PCS layers at any baud rate up to 16Gbps. The PMA is delivered as a hard macro while the fully-synthesizable soft PCS includes performing all necessary calibration and self-test functions. The universal PHY architecture allows forming arbitrarily wide efficient links by being independent of the need for a common CMU.



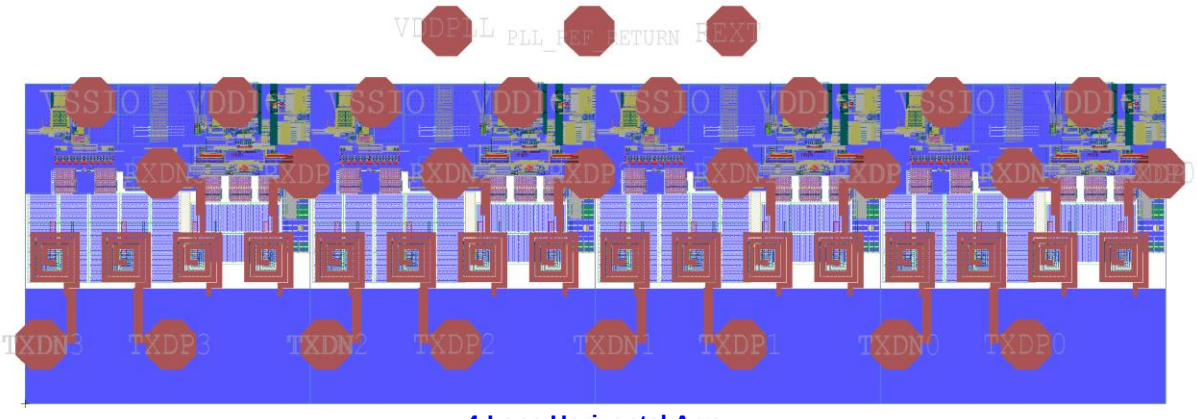
TX Eye Diagram & RX Jitter Tolerance at 16G



1-Lane PHY



4-Lane Vertical Array



4-Lane Horizontal Array

Multi-Array / Multi-Orientation SERDES Layout Examples (not to scale)
(PHY can be arrayed to support any number of lanes per link)