NEWS ALERT

Analog Bits to Present Papers on Wafer-Scale Sensors and PCIe Clock Systems at TSMC 2020 Open Innovation Platform® Ecosystem Forums

Santa Clara, CA, August 24, 2020 – Analog Bits (www.analogbits.com), a leading provider of low-power mixed-signal IP (Intellectual Property) solutions, will be presenting two ground-breaking papers at this year's TSMC Online Open Innovation Platform® (OIP) Ecosystem forums on August 25th.

Paper One: Case Study of AI Wafer Scale SoC from Cerebras Systems using Analog Bits Power Integrity Sensors

1. High-precision, high-sensitivity, small footprint sensors which can populate wafer scale SOC effectively and economically
2. Programmable, multi-threshold, cascadable sensors used to monitor all wafer level power and operations

Paper Two: Design & Integration of Complete On-die Clock Subsystem for PCIe Gen 5

1. On-die PCIe clock source for high-precision, low-jitter, and small footprint
2. Expanding PCIe Gen5 clock subsystem into other clocking needs, such as Ethernet

WHEN	*WHERE*	*REGISTER*
August 25th, 2020	**Both papers are available via TSMC Online Forums, under the HPC/3DIC track**	**https://tsmc-signup.pl-marketing.biz/attendees/2020symp/na/registration**

About Analog Bits

Founded in 1995, Analog Bits, Inc. (www.analogbits.com), is the leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SOCs. Products include precision clocking macros such as PLLs & DLLs, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's as well as specialized Sensors.

With billions of IP cores fabricated in customer silicon, from 0.35-micron to 7-nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

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