Media Alert:

Analog Bits Showcases Silicon of Analog and Mixed Signal IP Products on TSMC N7 Process Targeting Automotive Grade with Split Corner Lots and PVT Characterization Results Available

- Santa Clara, CA, September 26th, 2019 – Analog Bits (www.analogbits.com), an industry leading provider of low-power mixed-signal IP (Intellectual Property) solutions is demonstrating its silicon results targeting automotive grade for its analog and mixed signal IP products on TSMC's N7 process. The list of IPs includes wide range Integer PLL, Fractional PLL, Sensors, differential high speed IOs and Wide Frequency Range Oscillator Macro
- The complete family of analog and mixed-signal IPs, now with characterization report is immediately available for customer integration and tape-out.

WHAT: 7nm test chip silicon measurement targeting automotive grade:

Highlights of the Demo:

- 8 GHz PLLs for Integer and FracN
- 4 Gbps TX and RX IO's
- Wide Frequency Range Oscillator Macro
- Integrated Sensors

WHEN: September 26, 2019 (registration begins at 8:00am)

WHERE: TSMC 2019 Open Innovation Platform® Ecosystem Forum, Booth: 908, Santa Clara Convention Center, 5001 Great America Parkway, Santa Clara, CA 95054

Notice: The TSMC Open Innovation Platform® Ecosystem Forum is an invitation only event and all attendees should pre-register.

About Analog Bits: Founded in 1995, Analog Bits, Inc. (www.analogbits.com), is a leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SOCs. Products include precision clocking macros, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's and broad portfolio of Sensors. With billions of IP cores fabricated in customer silicon, from 0.35-micron to 5-nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

For more information, please contact: Will Wong 650-314-0200 will@analogbits.com