

Wide Range PLL DATASHEET



Features

- Electrically Programmable PLL for multiple applications
- Wide Ranges of Input and Output Frequency for diverse clocking needs
- Implemented with Analog Bits' proprietary architecture using core logic devices only
- Fully integrated inside industry standard's IO ring with proprietary low noise ESD structure
- Smallest PLL in the industry – occupies zero core area
- Lowest power consumption – less than 1mA
- Spread Spectrum tracking capability
- Uses no external on-chip components or band-gaps, minimizing power consumption
- Excellent jitter performance with optimized noise rejection

General Description

Analog Bits' wide range PLL addresses a large portfolio of applications, ranging from simple clock de-skew and non-integer clock multiplication to programmable clock synthesis for multi-clock generation. The PLLs are designed for digital logic processes and uses robust design techniques to work in noisy SoC environments, such as high speed communication to low power consumer to memory interfaces.

The PLL macro is implemented in Analog Bits' proprietary architecture that uses core devices only, removing constraints on the choice of IO devices within the standard logic process. The PLL is the smallest PLL in the industry and resides inside the IO ring of two analog power supply pads, occupying no core area. In order to minimize noise coupling, the PLL incorporates a proprietary ESD structure, which is proven in several generations of processes. Eliminating band-gaps and integrating all on-chip components such as capacitors and ESD structures, helps the jitter performance significantly and reduces stand-by power. The PLL macro fits into any industry standard IO pad pitch and is available for both staggered and in-line IO's.

Silicon Proven

Wide Range PLL macros from Analog Bits have been silicon proven in numerous 0.13u processes with 100% first time working PLL's.

Operational Limit of Wide Range PLL

Description	Symbol	Min.	Typ.	Max.	Units
Input frequency	FREF	5		200	MHz
Output frequency	FOUT	20		1000	MHz
Functional lock limits of input frequency	FREF	4		225	MHz
Output Duty Cycle, <500MHz	t _{DO}	45		55	%
Output Duty Cycle, >500MHz	t _{DO}	40		60	%
Lock Time	t _{LOCK}			100	us
Maximum Lock time			100µs@5MHz		
Total area of macro (e.g. 2 40u pad slots)	A		0.024		sq.mm
Chip core area requirement	CA		0		sq.mm
Total Power	I _{DD}		1		mA
Static Power, when Reset is asserted and inputs are quiescent	I _{DDQ}		<1		uA
Operational Voltage	V _{OP}	1.08	1.2	1.32	V
Operational Temperature	T _{OP}	0	25	125	C
Functional Temperature	T _{FUN}	-40C		125	C

Table 1 Operational Limit of Wide Range PLL

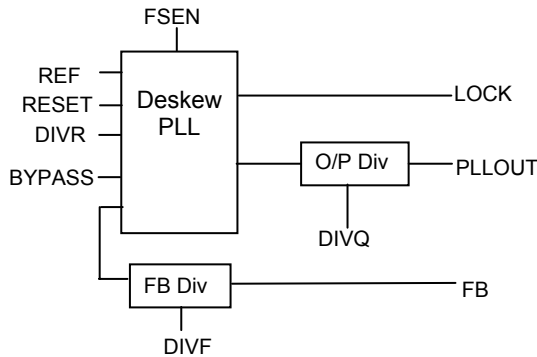


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Functional Diagram in PLL Mode



Functional Diagram Synthesizer Mode

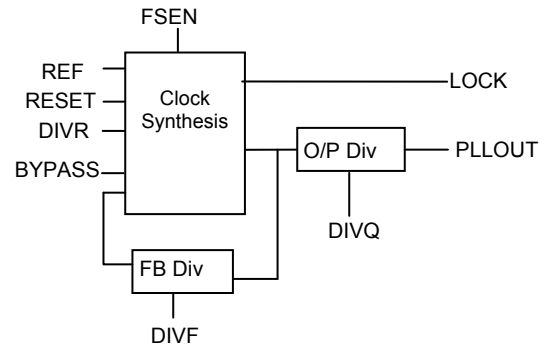


Figure 1 Pin Diagram and Modes of Operation of Wide Range PLL

Pin Description of Wide Range PLL

Pin	Type	Function
PLLOUT	Output	PLL Output
LOCK	Output	Lock Indicator Output
RESET	Input	PLL Internal Reset
BYPASS	Input	PLL Bypass enable
REF	Input	Reference Clock
FB	Input	Feedback Clock
DIVR []	Input	Reference Divider Value
DIVF []	Input	Feedback Divider Value
DIVQ []	Input	Output Divider Value
FSEN	Input	Frequency Synthesizer enable.
Note: All input port pins have antenna diodes		

Table 2 PLL Pin Descriptions

The phase-locked loop (PLL) block is provided as a drop-in functional block that fits in industry standard IO rings. The PLL can accept input frequencies from 5 MHz to 200 MHz. Because of the wide input frequency range and comprehensive divider options, several control bits are provided to set the operating mode of the PLL.

A LOCK signal is provided to indicate that the PLL has locked on to the incoming signal. A RESET control is provided to power down the PLL and reset it to a known state. A BYPASS signal is provided which both powers-down the PLL and bypasses it such that PLLOUT tracks REF. Either BYPASS or RESET may be used for power-down IDDQ testing.

For detailed product datasheet please contact sales@analogbits.com



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