



Features

- Integrated video PLL with Phase Interpolation and Coast
- Volume production at TSMC for high-end flat panel monitors
- Entire design uses standard core logic devices
- Uses external crystal reference for high PSRR
- Low Power Consumption, 150mW at 2.5V
- Low Area, <0.6 sq.mm.
- Programmable power vs. performance
- Programmable jitter rejection
- Excellent dynamic performance

General Description

Analog Bits Video Capture PLL macro is designed for applications that require precise clock generation from a highly noisy and low frequency input pulses, such as video slave and HDTV SoC. The core operates at a maximum pixel clock rate of 160MHz and uses only core devices and hence can be easily integrated into a digital SoC. The core is fully self-contained integrating all the required circuitry for generating a high-quality phase-variable pixel stream from a mediocre quality Hsync. In addition all of the required isolation from the digital section is incorporated to maintain the highest level of noise immunity. The PLL uses a system reference clock (e.g. 14.318MHz crystal) as a high precision time reference. The PLL utilizes a high-precision 28-bit digital frequency synthesizer, with a programmable all-digital loop filter making it possible to generate an output clock with less jitter than the typical Hsync reference, enabling the production of pixel clocks superior to that of an external analog PLL. Typical power consumption of the core is 150mW at 135MHz pixel rate. The core is also designed with programmable power adjustment to allow for power vs. performance tradeoffs.

Silicon Proven

This block has been Silicon Proven in the standard, 0.25um CMOS, Single Poly, 5 metal TSMC process and in volume production by high-end flat panel suppliers. 0.18um porting available upon request

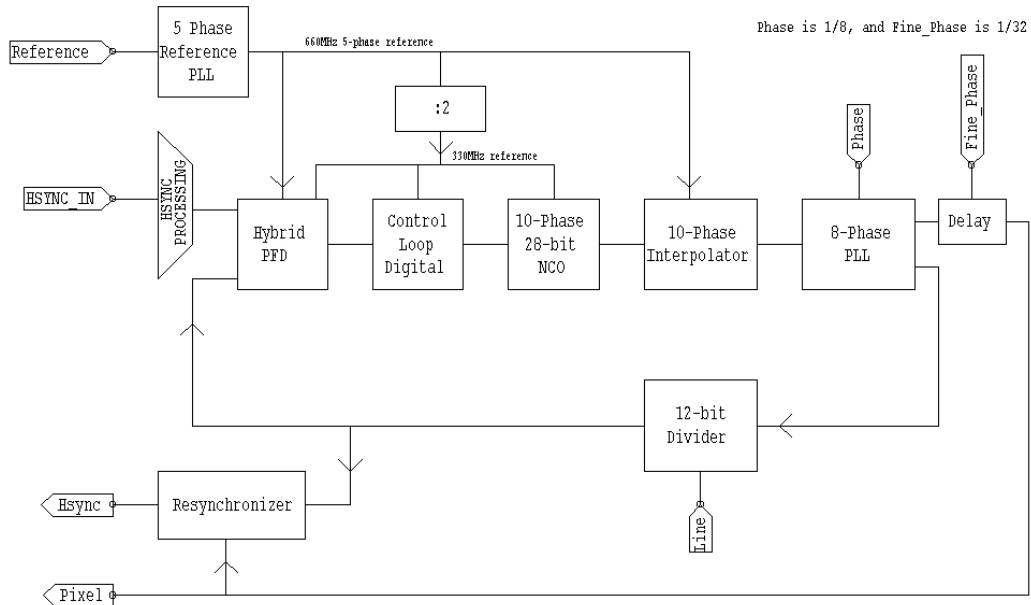
Key Specifications

Parameter	Value	Comments
Output Pixel Frequency	25MHz - 160MHz	Extended ranges available
Pixels per Line	700 – 2000	Extended ranges available
Input Hsync Frequency	25 – 100KHz	Extended ranges available
Output Jitter, short term, @160MHz	±125pS	
Output Jitter, long term, @160MHz	±450pS	
Power Supply (VDD)	2.3V to 2.7V	
Power Consumption	150mW	Vdd=2.5 & 135 MHz
Core Area	580 μM X 1020 μM	





Block Diagram



Electrical Characteristics

Parameter	Min	Typ	Max	Units
Power Supply	2.3	2.5	2.7	V
Analog Power Supplies	2.3	2.5	2.7	V
Junction Temperature	0		105	C
Supply Current		50		mA
Supply Current in power-down mode			20	uA
Area		0.6		sq.mm.
Pixel Divider Ratio (Pixels per line)	700		2000	
Input Clock Frequency	14.3	27.0	50	MHz
Input Hsync Frequency	25		100	KHz
Duration of Input Hsync Pulse	25		1500	nS
Subsequent Input Hsync Pulse Rejection Period	50			nS
Output Pixel Frequency	25		160	MHz
Output Duty Cycle	45	50	55	%
Output Jitter, short term (pixel period), @160MHz	-2		2	%
Output Jitter, short term (pixel period), @25MHz	-1		1	%
Output Jitter, long term, @160MHz	-450		450	pS
Output Jitter, long term, @25MHz	-600		600	pS
Time to Lock @65MHz pixel, 50KHz Hsync		500		Lines



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