HIGH SPEED TERNARY CAM

Features

- High speed ternary CAM for networking applications – 800+ Mega Look-ups Per Second
- Granular masking ability – bit, byte and word masks
- Independent look-ups of address available at speed every cycle
- Automatic resolution of multiple hits
- User selectable replacement algorithm offering high degree of flexibility
- Incorporates dynamic and pipelined techniques for low area and high speed
- Full custom design using standard logic process rules
- Optimized macro size to reduce power – 512 entries x 144 bits
- Independent 96 key bits for address matching with mask function and 48 bits of data
- Bankable architecture to increase search depth, with no performance loss
- Test options: Direct Entry Read, Early Hit Signal, Standby included

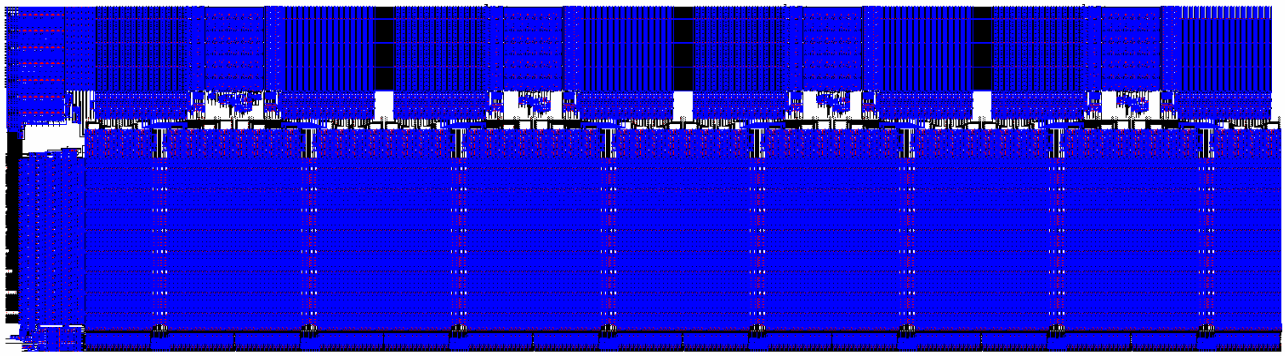
General Description

High speed network search engines used in high-end routers, Ethernet and ATM switches require high performance look-ups for address matching. A typical network search engine has an IP address that has to be matched to a physical address for high speed network processing. Such applications require sophisticated CAM arrays that are optimized for performance. Compiler generated CAM instances seldom meet the performance requirements.
Analog Bits has developed a unique full-custom Ternary CAM macro for TSMC CL013LV process that is capable of operating at 800+ MHz (worst-case). The CAM has 512 entries of 144 bits wide, consisting of 96 key bits size for address matching and 48 bits for data. High speed dynamic logic and pipelined techniques are used to boost performance and lower the area of the macro, performing single cycle address comparison and pipe-lined data access. The CAM is also provided with a granular mask function capability; masking can be down to every bit with options for byte and word masking. The CAM macro has the ability to automatically resolve conflicts upon multiple hits return only one unique result. Multiple hit and Early Hit flag assertion allow system designers to optimize performance. The CAM is designed using careful full-custom transistor design techniques and use standard logic rule decks, avoiding needs for redundancy to improve yields. Care is taken to greatly reduce power, consuming less than 0.5mA/MHz. The CAM is also equipped with diagnostic capability such as Direct Read (as opposed to operational match-read) and standby mode.

Silicon Proven

800MHz CAM macro is proven in silicon and available in TSMC CL013LV/LVOD process

Analog Bits CAM Macro in TSMC CL013LV/LVOD Process



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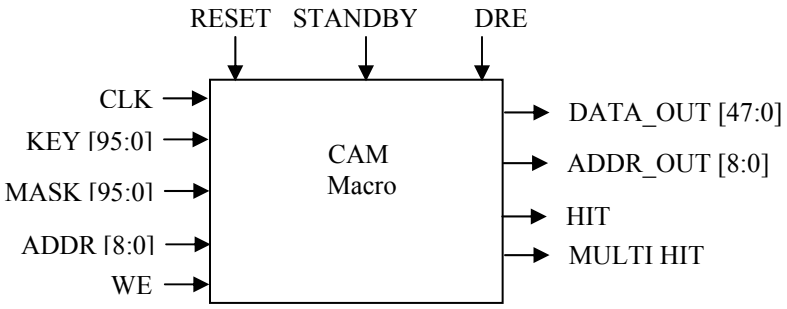
Pin Diagram



Pin Description

Pin	Type	Description
CLK	Input	CAM Clock
KEY [95:0]	Input	96 bit Key bits
MASK [95:0]	Input	96 bit Mask bits for each Key Bit
ADDR [8:0]	Input	Write and Direct Read Address
WE	Input	Write Enable (Active High) to enable direct write
DRE	Input	Direct Read Enable for debugging
RESET	Input	Resets the CAM array
DATA_OUT [47:0]	Output	48 bits of data
ADDR_OUT [8:0]	Output	Entry location of hit
STANDBY	Input	Powers down the CAM
HIT	Output	Indicates a match or no-match
Multi Hit	Output	Multi-hit flag indicator

CAM Operation

Operation	Description
CAM WRITE	For writing to the CAM, data is to be provided on both the “key” bus and “mask” bus. The “key” 96 bits will be for internal “key” value, and the 48 LSBs of the “mask” bus will be for “data”. The WE (Write Enable) signal must be high and the ADDRESS[8:0] must be valid for the write cycles
CAM READ (Normal Access)	For reading the CAM, the “key” will be provided on the 96 bit bus, and a “mask” will be provided on another 96 bit bus. Only the “key” bits with the corresponding “mask” bits asserted will be compared in the CAM. If there is a match then in the subsequent cycles any multiple hit issues are resolved, then the data is accessed, and then the data is presented to the output pins. The “data” and “index” bits are output with “match” and “multiple match” status signals. The CAM automatically resolves any multiple hit issues, and presents the lowest addressed entry.
CAM DIRECT READ (Option)	For Direct Read (as opposed to operational match-read) of the CAM, the DRE (Direct Read Enable) signal must be high, and the ADDRESS[8:0] must be valid (same as the address bus for write). The data will appear on the regular data_out bus as though the addressed line were the only hit.
CAM STANDBY	A STANDBY signal is available to the CAM. It should be asserted when STANDBY is required, and de-asserted a clear cycle before CAM operations re-commence. It must not be asserted while a WRITE is in progress. Its assertion will immediately invalidate any reads in progress.

Area, Performance and Power Specifications for CAM in TSMC CL013LV Process

Array Size	Speed	Area	Power
512 entries x 144 bits	800 MHz (worst case)	520u x 1991u	0.5mA/MHz (worst case)