

HIGH SPEED DUAL PORT SRAM



Features

- Processor class pipelined high speed register files – 800MHz+
- 2 address ports that can be operated as read or write ports
- Fully synchronous with pipelined or zero latency option data outputs
- Low voltage data retention
- Byte-write option available
- Incorporates dynamic and pipelined techniques for low area and high speed
- Full custom design using standard logic process rules and logic rule based 8T cell
- Optimized macro size to reduce power and increase speed – 1K or 512 or 256 deep
- Wide output bus up from 40 bits to 128 bits
- Parity included in wide word outputs
- Bankable architecture that easily tiles to increase register file size
- Over macro routing on M6+ metal layers with no performance degradation

General Description

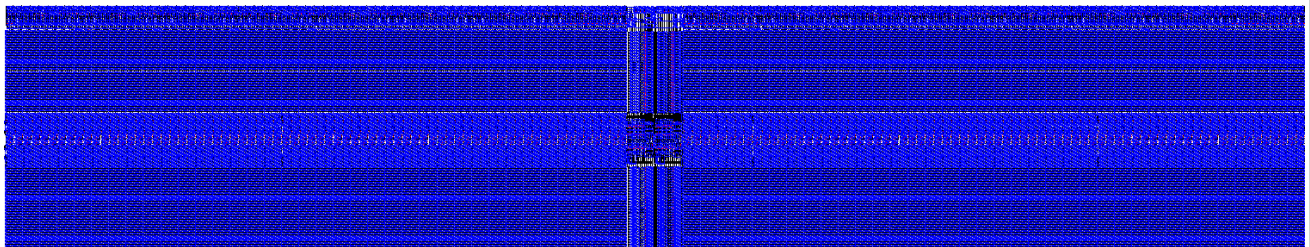
Speeds of network processor or high-speed CPU machines are highly dependant on performance of Dual Port SRAM's. Applications for Dual Port SRAM's include high speed register files, high speed FIFO's and typical network processors have between 25 to 50 instances of these macros scattered along the area of the chip. Speed and power of these macros are a critical parameter that controls the system performance. Commodity compilers supporting standard logic processes for foundries, fail to address processor class designs performance needs.

Analog Bits has developed a family of full-custom Dual Port SRAM macros for TSMC CL013LV process that is capable of operating at 800+ MHz (worst-case). This Dual Port SRAM's are available in multiple word depths from 256, 512 or 1K words and varying data-widths from 40 bits to 128 bits. The larger word widths support internal parity for error detection. Each address ports can perform read and write operations, allowing 2R, 2W or 1R/1W in a given cycle. High speed dynamic logic and pipelined techniques are used to boost performance and lower the area of the macro, performing either a single cycle read operation at 500MHz or pipe-lined data access at 800MHz. The Dual Ports use standard logic rules with a full-custom 8T bit cell that is optimized for performance, improving the yield and eliminating needs for redundancy schemes. The macros are designed to robustly work in a noisy SoC environment – over routing on higher layers of metals such as M6 or physical proximity to high speed blocks does not degrade performance. Macros also support such as byte writes to save clock cycles for operations such as read-modify-writes. The macros are easily bankable to increase array sizes and support a true register file style layout by having address ports reside on the same side of the macro

Silicon Proven

800MHz+ pipelined or 500MHz+ zero-latency SRAM macros are proven in silicon and available in TSMC CL013LV/LVOD process

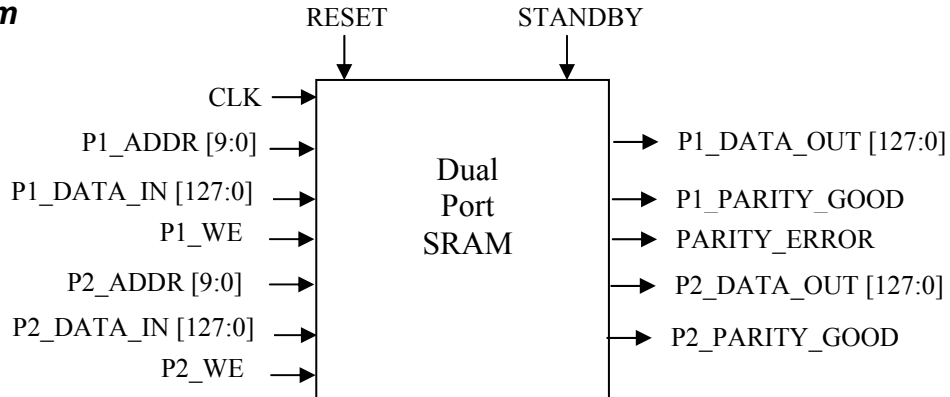
Analog Bits Dual Port SRAM Macro in TSMC CL013LV/LVOD



HIGH SPEED DUAL PORT SRAM



Pin Diagram



Pin Description

Pin	Type	Description
CLK	Input	SRAM Clock
P1_ADDR [9:0]	Input	Read and Write Address for Port 1
P2_ADDR [9:0]	Input	Read and Write Address for Port 2
P1_DATA_IN [143:0]	Input	Write Data for Port 1
P2_DATA_IN [143:0]	Input	Write Data for Port 2
P1_WE	Input	Write Enable (Active High) for Port 1
P2_WE	Input	Write Enable (Active High) for Port 2
P1_DATA_OUT [127:0]	Output	128 bits of output data from Port 1 including parity
P1_PARITY_GOOD	Output	Flag to indicate if parity matched for Port 1
P2_DATA_OUT [127:0]	Output	128 bits of output data from Port 2 including parity
P2_PARITY_GOOD	Output	Flag to indicate if parity matched for Port 2
PARITY_ERROR	Output	Flag to indicate Parity Error on Port 1 or Port 2
RESET	Input	Resets the SRAM array
STANDBY	Input	Powers down the SRAM

SRAM Operation

Operation	Description
SRAM WRITE	The WE input for each port controls the write or read activity of the corresponding ports. Address and data are set-up prior to rising edge of the clock and write will occur when the WE is high. Write is completed in one cycle
SRAM READ	Read address is set-up prior to the rising edge of the clock, and WE are low. Pipelined read data will be available in subsequent clock cycle (1 cycle latency) Zero latency read data will be available in the same cycle of the clock
RAM STANDBY	A STANDBY signal is available to the SRAM. It should be asserted a clear cycle before STANDBY is required, and de-asserted a clear cycle before RAM operations recommence. Its assertion will invalidate any reads in progress.

Area, Performance and Power Specifications for TSMC CL013LV Process

Array Size	Speed	Area	Power
1K x 128 bits	Pipelined: 800 MHz Zero Latency: 500MHz	2.72mm x 0.46mm	0.3mA/MHz (worst case)



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