

HIGH SPEED SINGLE PORT SRAM



Features

- Processor class pipelined high speed SRAM – 800MHz+
- Fully synchronous with pipelined or zero latency option data outputs
- Built-in redundancy for yield improvements
- User selectable redundancy schemes configured externally to SRAM
- Low voltage data retention
- Byte-write option available
- Incorporates dynamic and pipelined techniques for low area and high speed
- Full custom design using standard logic process rules and 6T bit cell
- Optimized macro size to reduce power and increase speed – 4Kx144
- Data outputs support Error Correction Code (ECC) for 128 bits
- Bankable architecture that easily tiles to increase SRAM size
- Over macro routing on M6+ metal layers with no performance degradation

General Description

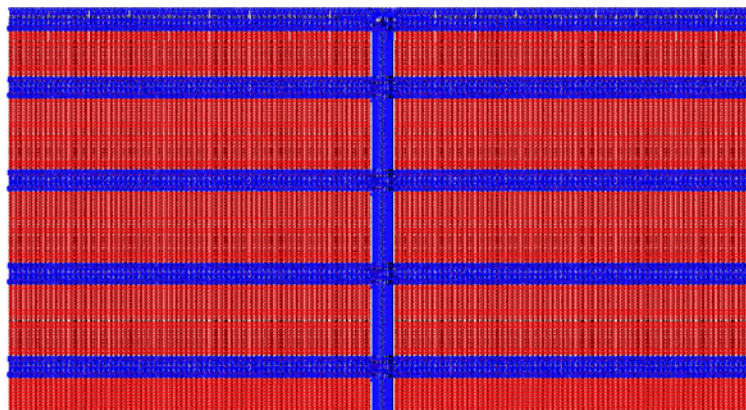
Speeds of network processor or high-speed CPU machines is highly dependant on performance of on-chip cache SRAM's. Traditional IDM and processor design teams, have internal expertise to design the highest performing SRAM for their specific application needs. Commodity compilers supporting standard logic processes for foundries, fail to address processor class designs performance needs. Designing high-speed processor class SRAM's requires a deep understanding of system and transistor design.

Analog Bits has developed a family of full-custom SRAM macros for TSMC CL013LV process that is capable of operating at 800+ MHz (worst-case). A typical SRAM size is 4K bits deep and 144 bits wide, supports a 128 bits data-with 16 bits of data for an external ECC. High speed dynamic logic and pipelined techniques are used to boost performance and lower the area of the macro, performing either a single cycle read operation at 500MHz or pipe-lined data access at 800MHz. The design uses standard yield proven foundry bit cells, incorporating row redundancy for up to 8 rows of replacement. Designers have the choice of using redundancy schemes such as laser or electrical fuses, or software control registers external to the SRAM macro. The macros are designed to robustly work in a noisy SoC environment – over routing on higher layers of metals such as M6 or physical proximity to high speed blocks, does not degrade performance. Macros also support such as byte writes to save clock cycles for operations such as read-modify-writes. The macros are easily bankable to increase array sizes.

Silicon Proven

800MHz+ pipelined or 500MHz+ zero-latency SRAM macros are proven in silicon and available in TSMC CL013LV/LVOD process

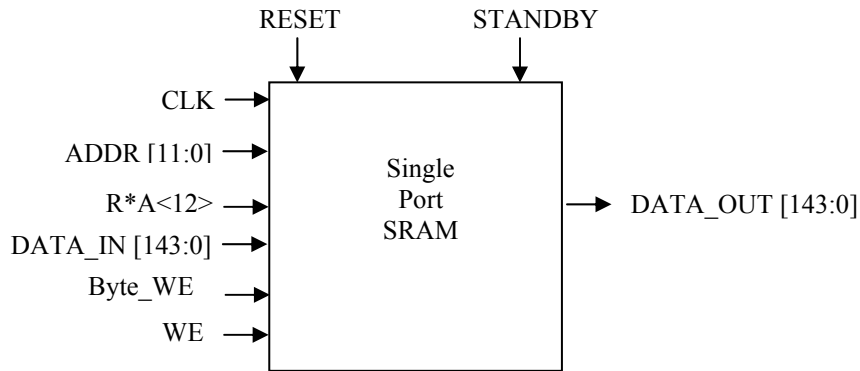
Analog Bits 1P SRAM Macro in TSMC CL013LV/LVOD



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Pin Diagram



Pin Description

Pin	Type	Description
CLK	Input	SRAM Clock
ADDR [11:0]	Input	Read and Write Address
R*A [12]	Input	Redundant address for replacement up to 8 rows
DATA_IN [143:0]	Input	Write Data
WE	Input	Write Enable (Active High)
Byte WE	Input	Write Enable for Byte Writes
DATA_OUT [143:0]	Output	144 bits of output data from RAM with option to support ECC
RESET	Input	Resets the SRAM array
STANDBY	Input	Powers down the SRAM

SRAM Operation

Operation	Description
SRAM WRITE	The WE input controls the write or read activity. Address and data are set-up prior to rising edge of the clock and write will occur when the WE is high. Write is completed in one cycle
SRAM READ	Read address is set-up prior to the rising edge of the clock, and WE is low. Pipelined read data will be available in subsequent clock cycle (1 cycle latency) Zero latency read data will be available in the same cycle of the clock
RAM Redundancy	SRAM is provided with 8 rows of redundant address. An input bus R*A<11'4> will be provided to address each of the 8 row groups to be replaced (*in R*A is 0 through 7), with a corresponding control signal R*A<12> to enable each replacement. The control of the redundancy feature is external to the SRAM macros, providing flexibility to the user on the schemes of redundancy
RAM STANDBY	A STANDBY signal is available to the SRAM. It should be asserted a clear cycle before STANDBY is required, and de-asserted a clear cycle before RAM operations recommence. Its assertion will invalidate any reads in progress.

Area, Performance and Power Specifications for TSMC CL013LV Process

Array Size	Speed	Area	Power
4K x 144 bits	Pipelined: 800 MHz Zero Latency: 500MHz	1.725mm x 1.42mm	0.2mA/MHz (worst case)



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