



## Features

- Generates precise degrees of clock phase shifting for high speed DDR/QDR
- Phase adjustments of non-continuous strobe clocks
- Compensates for external clock and data delays
- Programmable delay for precise and granular control of delay
- Quick stop/re-start capability for power management
- Uses Analog Bits proprietary architecture that uses core logic devices only
- Fully integrated inside IO ring with proprietary low noise ESD structure
- Uses no external on-chip components or band-gaps minimizing power consumption
- Excellent jitter performance with optimized noise correction
- Fits into any IO ring with appropriate filler cell option

## General Description

Digital IC's that interface to high speed memory interfaces such as DDR/QDR receive data and strobe clocks simultaneously. In order to ensure timing and guarantee data-capture, the incoming clocks need to be phase adjusted, typically by 90 degrees. In addition, the strobe clocks appear non-continuously as a method of reducing switching power and hence will require a clock system generation macro to rapidly generate clocks

Analog Bits DLL macro generates a 90 degree delayed clocks (optionally 180 or 360 degrees) from non-continuous clock strobe. The macro also has a built-in stop capability that allows powering down the analog portions when the incoming clock is idling saving power. Additionally the macro has the ability to perform rapid re-start the clocks with the incoming clocks. The macro is also provided with programmable gate-delays which can be used to compensate for external data-path or clock-tree delays. The DLL uses our proprietary architecture proprietary ESD structure that uses core devices only, and resides inside the IO ring of two analog power supply pads, occupying no core area. The DLL macros fit into any standard IP pad pitch and can also be integrated to any custom IO rings.

## Silicon Proven

DLL is silicon proven in several 0.13u processes including TSMC and UMC. Porting to Chartered and IBM fabs upon request.

## Electrical Properties

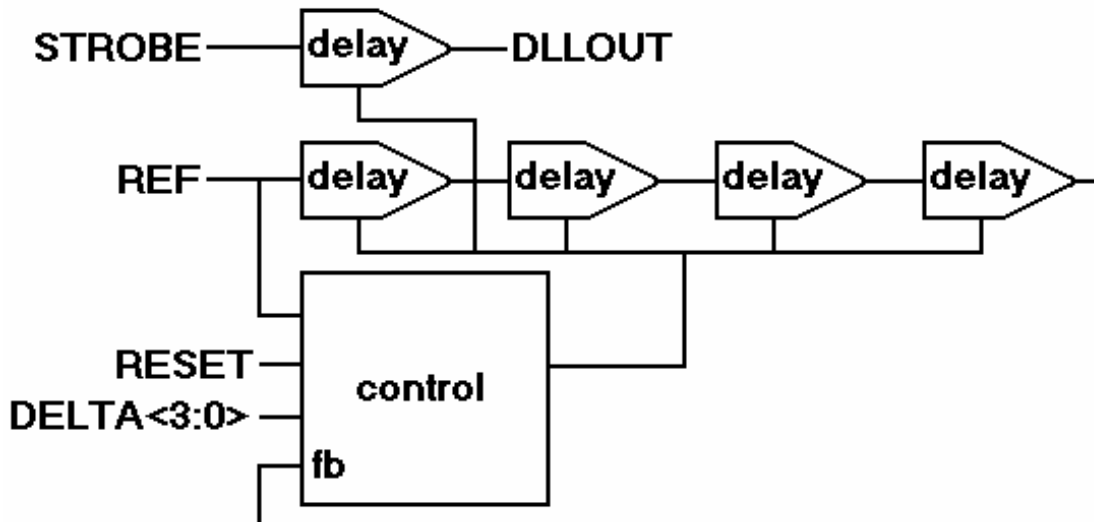
Parameter	Units	Min	Typ	Max	Comment
Reference Frequency	MHz	50		200	Frequency of REF. STROBE may be slower.
Reference Duty Cycle	%	40		60	
Strobe Pulse Width	nS	2			low and high
Duty Cycle Degradation	%	-2%		+2%	
Lock Time	Cycles			512	cycles of input reference clock from RESET
Lock Time	Cycles		0		cycles of input reference clock from coasting
Static Phase Error	pS	-100		+100	DLLOUT rising edge phase error at 200MHz
Cycle to Cycle Jitter	pS	-50		+50	With constant reference frequency and analog grade power supply
Analogue Power	mA		10		Unloaded @200MHz
Static Power	uA		<1		Leakage current only when reset is asserted, the inputs are quiescent and no output load.



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**Functional Diagram of DLL**



**Pin Description**

Pin	Type	Description
VDDA	Power	Pad connection for analogue power.
VSS	Power	Pad connection for analogue power filter
REF	Input	Reference Clock, active on rising edge.
DLL OUT	Output	90° phase delay of reference clock period.
RESET	Input	Resets DLL control when high, initializes delay stages to minimum delay, and powers-down analogue components.
STROBE	Input	Source clock for DLL OUT
DELTA<3:0>	Inputs	Adjusts the DLL OUT phase by small gate delays, which may be used to compensate for external datapath delays. DELTA3 is a sign bit, and DELTA2, DELTA1, DELTA0 are a binary gate delay quantity.

**Optional Enhancements to DDR-DLL**

- Higher frequency option available for next generation DDR up to 350MHz/700Mb/s
- Dual slave path options for alternate strobe schemes
- Customizable options for specified pad rings



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