Join us at the 2016 Design Automation Conference (DAC)

See a Demonstration of Analog Bits' latest IP in TSMC 16FFC

Leading low power IP provider to showcase Sensor & PLL IP products in TSMC's latest 16FF process

Austin, TX, June 6, 2016 – Analog Bits (www.analogbits.com) will be demonstrating the latest low power physical IP at this year's Design Automation Conference in Austin, TX from June 6-8. Setting the standard with their half-power SERDES (Serializer/Deserializer), Analog Bits will now be demonstrating their latest PVT Sensor (Process, Voltage, Temperature) and PLL products in TSMC's latest 16nm process called 16FFC. Analog Bits continues to change the way the semiconductor industry uses mixed-signal IP through a sharp focus on low power, flexible use and first-time right design practice. Analog Bits' products have shipped in billions of devices and are supported across a wide variety of process geometries.

WHAT: **Analog Bits' latest IP solutions in TSMC's 16FFC process**

WHEN: **Design Automation Conference (DAC) 2016**
Exhibits: June 6-8, 2016

WHERE: **Analog Bits booth #644**
Austin Convention Center
500 East Cesar Chavez Street
Austin, TX 78701

About Analog Bits: Founded in 1995, Analog Bits, Inc. (www.analogbits.com), is the leading supplier of mixed-signal IP with a reputation for easy and reliable integration into advanced SOCs. Products include precision clocking macros such as PLLs & DLLs, programmable interconnect solutions such as multi-protocol SERDES and programmable I/O's as well as specialized memories such as high-speed SRAMs and TCAMs. With billions of IP cores fabricated in customer silicon, from 0.35-micron to 16/14-nm processes, Analog Bits has an outstanding heritage of "first-time-working" with foundries and IDMs.

For more information, please contact:

Will Wong
650-314-0200
will@analogbits.com