

Temperature Sensor Datasheet (28nm)



General Description

Analog Bits' temperature sensor is a highly integrated macro for monitoring temperature variation on-chip, allowing very high precision even in untrimmed usage. It consumes very little power even in operational mode, and leakage power only when temperature measurement is complete. The block includes a simple-to-use digital interface that works with standard core and IO level power supplies. The macro uses core and thick-oxide devices.

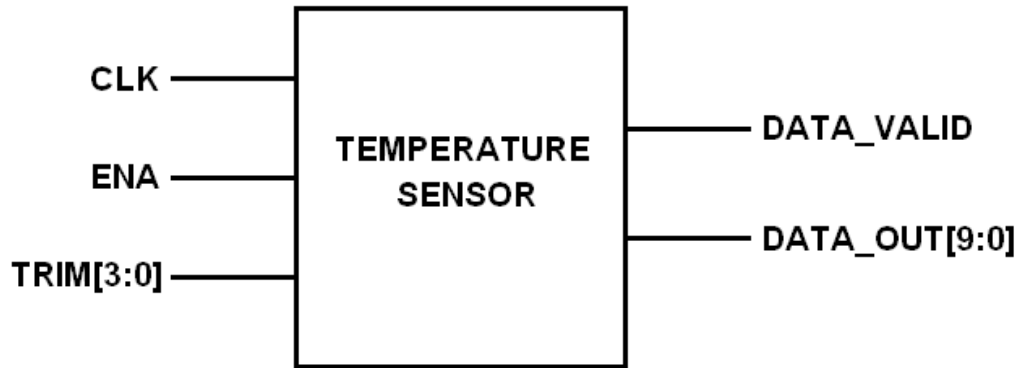


Figure 1: Temperature Sensor Block Diagram

Specifications

Description	Units	Min	Typ	Max
Accuracy (over range of 0°C to 125°C – post-trim)	°C		±1	
Accuracy (over range of 0°C to 125°C – untrimmed)	°C		±4	
Clock Frequency	MHz	0.5		1
Sample Rate (@1MHz CLK)	Samples/sec			50
Area	sq.mm		0.04	
Dynamic Power (@1MHz CLK, average)	µA		100	
Operating Voltage (Digital) (core voltage options: 0.85V, 0.9V, 1.0V)	V _{DIG}	0.765 0.8 0.9	0.85 0.9 1.0	0.935 1.0 1.1
Operating Voltage (Analog)	V _{ANA}	1.62	1.8	1.98
Operational Temperature	°C	0	25	125

Table 1: Temperature Sensor Specifications



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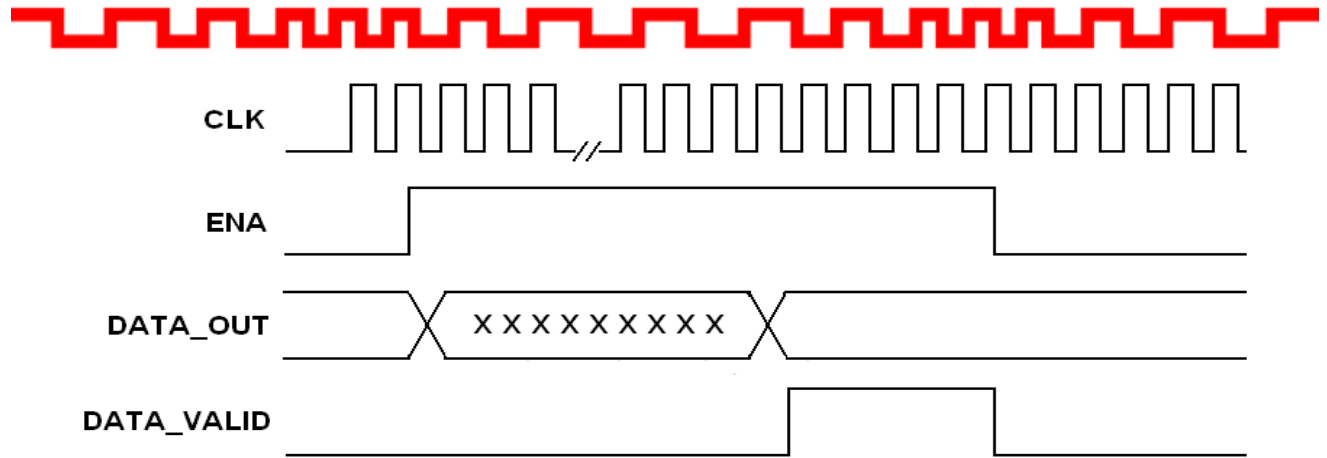


Figure 2: Timing Diagram

Pin Description

Pin	Type	Function
CLK	Input	A logic clock to run the digital portion of the temperature sensor. The actual speed is not very critical, and may be divided off of any convenient logic clock.
ENA	Input	A control signal commanding the temperature sensor to re-evaluate the local die temperature
TRIM[3:0]	Input	Optional programmable inputs which may be used to improve the absolute accuracy of the temperature sensor. The optimal values may be ascertained during test, or at any other time.
DATA_VALID	Output	An output signaling when the temperature sensing is complete, and when the sensor is available to re-assess the temperature.
DATA_OUT[9:0]	Output	A 10-bit bus representing the sensed temperature

Note: All input port pins have antenna diodes

Table 2: Pin Description

Deliverables and EDA Design Views

Front-end Design Views (with NDA)	Back-end Design Views (with License Agreement)
Verilog Model	GDSII stream file
Synopsys (LIB)	CDL/Spice netlist
Footprint (LEF) format	Application Notes inclusive of design integration guidelines (PDF)
Datasheet (PDF)	

Table 3: List of Deliverables