

4096 x 128 Ternary CAM Datasheet (28nm)



Features

- High speed ternary CAM for networking applications – 800 Mega Look-ups Per Second
- Granular masking ability – bit, byte and word masks
- Independent look-ups of address available at speed every cycle
- Automatic resolution of multiple hits
- User selectable replacement algorithm offering high degree of flexibility
- Incorporates dynamic and pipelined techniques for low area and high speed
- Full custom design using standard logic process rules
- Optimized macro size to reduce power – 4096 entries x 176 total bits
- Independent 128 key bits for address matching with mask function and 48 bits of data
- Test options: Direct Entry Read, Early Hit Signal, Standby included
- Global and Per-entry mask

General Description

High speed network search engines used in high-end routers, Ethernet and ATM switches require high performance look-ups for address matching. A typical network search engine has an IP address that has to be matched to a physical address for high speed network processing. Such applications require sophisticated CAM arrays that are optimized for performance. Compiler generated CAM instances seldom meet the performance requirements.

Analog Bits provides a unique full-custom Ternary CAM macro that is capable of operating at 800 MHz (worst-case). The CAM has 4096 entries of 176 bits wide, consisting of 128 key bits size for address matching and 48 bits for data. A Mask entry is available for each Key entry on a per-bit basis. A Valid bit is available for each Key and Mask entry. High speed dynamic logic and pipelined techniques are used to boost performance and lower the area of the macro, performing single cycle address comparison and pipe-lined data access. The CAM is also provided with a granular mask function capability; masking can be down to every bit. The CAM macro has the ability to automatically resolve conflicts upon multiple hits and return the highest priority result (lowest entry). Multiple Hit and early Hit flag assertion allow system designers to optimize performance. The CAM is designed using careful full-custom transistor design techniques and use standard logic rule decks, avoiding needs for redundancy to improve yields. Care is taken to greatly reduce power. The CAM is also equipped with diagnostic capability such as Direct Read (as opposed to operational match-read) and standby mode.

TCAM Specifications

Parameter	Unit	Min	Typ	Max	Comment
Entries	-		4096		
Match Width	-		128		
Lookup Width	-		48		
Input Clock	MHz	0		800	
Lookups per second (LUP/s)	MHz			200	Slow Sync mode (HIGH_SPEED=0)
				800	High Speed mode (HIGH_SPEED=1)
Total Area	sq.mm		2.8		
Operating Voltage	V	0.765	0.85	0.935	(core voltage options: 0.85V, 0.9V, 1.0V)
		0.81	0.9	0.99	
		0.9	1.0	1.1	
Operational Temperature	°C	-40	25	125	

Other TCAM configuration sizes available upon request

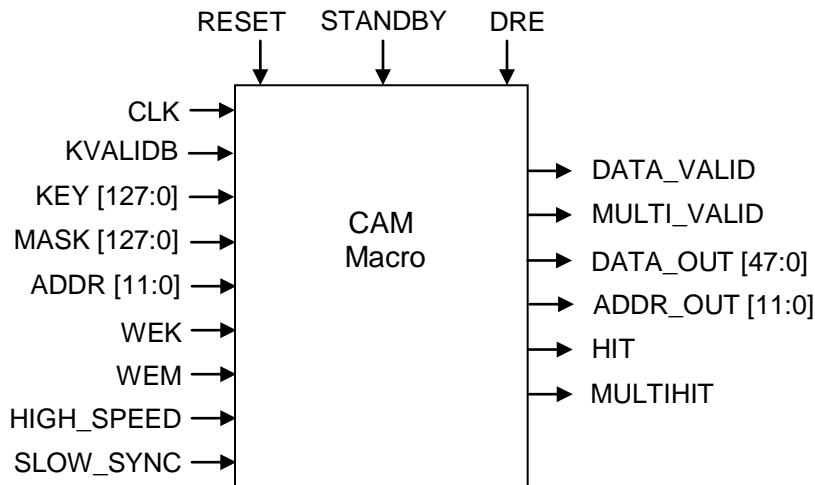


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Pin Diagram



Pin Description

Pin	Type	Description
CLK	Input	CAM Clock
KVALIDB	Input	Valid bit for Key entry (0 = Valid, 1 = Invalid)
KEY [127:0]	Input	128 bit Key bits, written for each Key entry
MASK [127:0]	Input	128 bit Mask bits, written for each Mask entry (0 = Compared, 1 = Masked)
ADDR [11:0]	Input	Write and Direct Read Address
WEK	Input	Write Enable Key (Active High) to enable direct write
WEM	Input	Write Enable Mask (Active High) to enable direct write
DRE	Input	Direct Read Enable for debugging
RESET	Input	Resets the CAM array
STANDBY	Input	Powers down the CAM
DATA_OUT [47:0]	Output	48 bits of data
ADDR_OUT [11:0]	Output	Entry location of hit
DATA_VALID	Output	Flags that data on DATA_OUT is the valid result of a current match. DATA_VALID is a delayed HIT signal synchronized to DATA_OUT.
MULTI_VALID	Output	A delayed MULTIHIT signal synchronized to DATA_OUT
HIT	Output	Indicates a match or no-match
MULTIHIT	Output	Multi-hit flag indicator
HIGH_SPEED	Input	When asserted makes LU rate equal to the clock frequency When de-asserted makes LU rate limited to ¼ of the clock frequency
SLOW_SYNC	Input	Input synchronization signal when HIGH_SPEED = 0. SLOW_SYNC should be high only for the clock rising edge before an access begins.



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