

Custom Programmable Low Power SERDES (28nm)

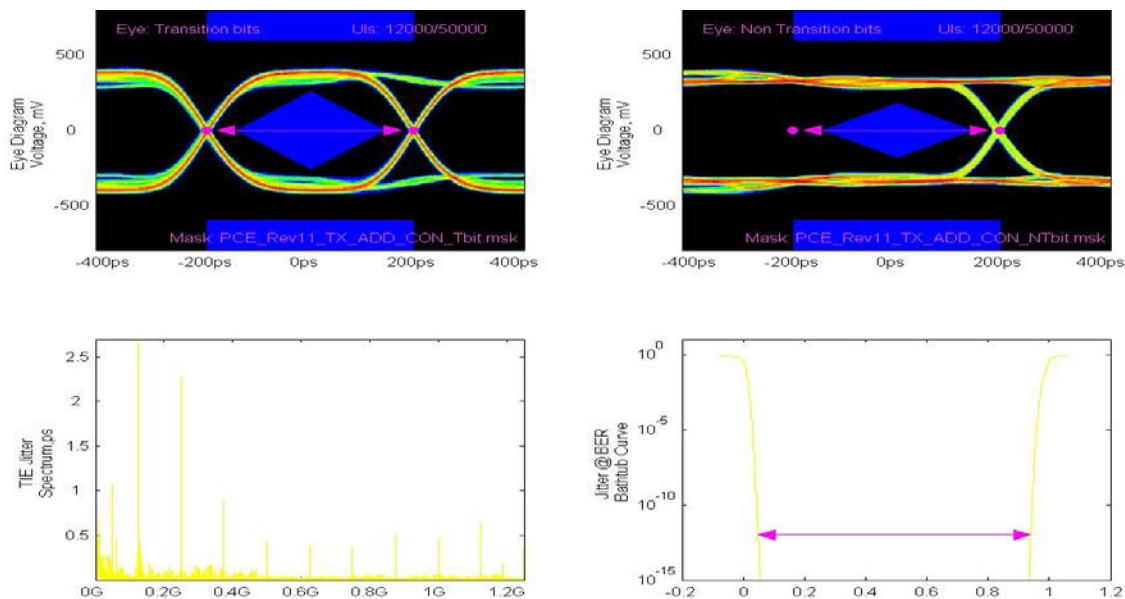


Features

- Programmable SERDES analog front end that supports 1 to 16+ Gbps standard serial protocols
- Supports SONET class jitter and Display SERDES applications
- Compact form factor – 0.095 mm² active silicon area per lane including ESD
- Industry leading low power – typically 4.3 mW/Gbps including termination
- Minimal latency – 3 UI between parallel transfer and serial transmission
- Single-lane macro scalable to unlimited link width – x1, x2, x4, x8, x16, etc.
- Finely configurable driver impedance, amplitude and 3-tap pre-emphasis
- Finely configurable receiver impedance, CTLE gain and bandwidth, and DFE
- Selectable parallel data bit widths such as 5, 8, 10, 16, 20
- Test support features such as ac-JTAG, near-end loopback, PLL bypass modes, etc.
- Protocol-compatible features such as beacon, Tx detect Rx, LOS, squelch, independent Tx/Rx rate, power modes, etc.
- Low pin-count and suitable for a variety of flip-chip and wire-bond packages
- Metallization scheme and pad/bump structures customizable to specifications
- Available with PCS to provide PIPE compatible PCI-Express Gen1/Gen2/Gen3 PHY solution

General Description

Analog Bits' Programmable SERDES provides a Physical Media Attachment (PMA) Layer capable of signaling at multiple data rates and supports multi-protocol market needs including a wide range of ac-coupled high-speed serial communication standards requiring serial Clock Data Recovery (CDR). The pin-configurable macro uses standard logic process devices, and exhibits exceptional input sensitivity, input jitter tolerance and low output jitter. Analog Bits' proprietary and industry leading PLL technology in combination with sophisticated circuit techniques and innovative IO design makes this macro an extremely area and power efficient solution. The PMA can be integrated with the available PCS to provide a PCI-Express Gen1/Gen2/Gen3 PHY solution, and has interface capability to allow integration with other customer-designed serial protocol PCS layers.



Example PCI Express Compliance Pattern BER Test



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