

Wide Range PLL Datasheet (28nm)



Features

- Electrically Programmable PLL for multiple applications
- Wide Ranges of Input and Output Frequency for diverse clocking needs
- Implemented with Analog Bits' proprietary architecture
- Fully integrated inside customer-specified IO ring
- Occupies no core area
- Low power consumption
- Spread Spectrum tracking capability
- Requires no additional on-chip components or band-gaps, minimizing power consumption
- Excellent jitter performance with optimized noise rejection

General Description

Analog Bits' Wide Range PLL addresses a large portfolio of applications, ranging from simple clock de-skew and non-integer clock multiplication to programmable clock synthesis for multi-clock generation. The PLLs are designed for digital logic processes and use robust design techniques to work in noisy SoC environments, such as high speed communication to low power consumer to memory interfaces.

The PLL macro is implemented in Analog Bits' proprietary architecture that uses core and IO devices. The PLL resides inside the IO ring that includes two analog power supply pads, occupying no core area. In order to minimize noise coupling and maximize ease of use, the PLL incorporates a proprietary ESD structure, which is proven in several generations of processes. Eliminating band-gaps and integrating all on-chip components such as capacitors and ESD structures, helps the jitter performance significantly and reduces stand-by power. The PLL macro fits into any standard IO pad pitch and can be implemented in staggered and in-line IO configurations.

PLL Operational Range

Description	Symbol	Min	Typ	Max	Units
Input Frequency	F_{REF}	10		600	MHz
Post-Divide Reference frequency	F_{PFD}	10		200	MHz
VCO Frequency	F_{VCO}			4000	MHz
Output Frequency	F_{OUT}	30		2000	MHz
Output Duty Cycle	t_{DO}	45		55	%
Total area of macro (excluding bond pad area) May vary depending on size of IO slots	A		0.02		sq. mm
Chip core area requirement	CA		0		sq. mm
Total Power	I_{DD}		4		mA
Operational Voltage (Digital) (core voltage options: 0.85V, 0.9V, 1.0V)	V_{DIG}	0.765 0.81 0.9	0.85 0.9 1.0	0.935 0.99 1.1	V
Operational Voltage (Analog)	V_{ANA}	1.62	1.8	1.98	V
Operational Temperature	T_{OP}	-40C	25	125	C

Table 1: PLL Operational Range

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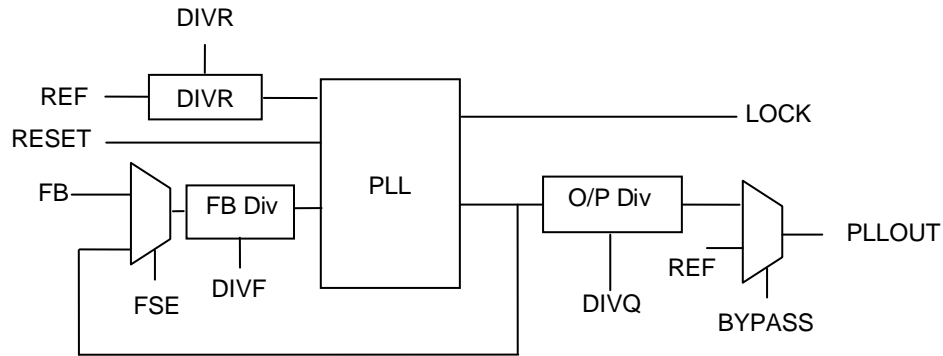


Figure 1: PLL Block Diagram

PLL Pin Description

Pin	Type	Function
PLLOUT	Output	PLL Output
LOCK	Output	Lock Indicator Output
RESET	Input	PLL Internal Reset
BYPASS	Input	PLL Bypass enable
REF	Input	Reference Clock
FB	Input	Feedback Clock
DIVR	Input	Reference Divider Value
DIVF	Input	Feedback Divider Value
DIVQ	Input	Output Divider Value
FSE	Input	Frequency Synthesizer enable

Note: All input port pins have antenna diodes

Table 2: PLL Pin Description

The phase-locked loop (PLL) block is provided as a drop-in functional block that fits in industry standard IO rings. The PLL accepts a wide range of input frequencies and can produce a wide range of output frequencies, as described in Table 1. Several control bits are provided to configure the desired operating mode of the PLL.

A LOCK signal is provided to indicate that the PLL has locked on to the incoming signal. A RESET control is provided to power down the PLL and reset it to a known state. A BYPASS signal is provided which both powers-down the PLL and bypasses it such that PLLOUT tracks REF. Either BYPASS or RESET may be used for power-down IDDQ testing.

Deliverables and EDA Design Views

Front-end Design Views (with NDA)	Back-end Design Views (with License Agreement)
Verilog Model	GDSII stream file
Synopsys (LIB)	CDL/Spice netlist
Footprint (LEF) format	Application Notes inclusive of design integration guidelines (PDF)
Datasheet (PDF)	

Table 3: List of Deliverables

Custom higher performance, video class and lower power versions available upon request.



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