

DDR3-2133 Compatible I/O Buffer (28nm)



Features

- High-Speed Bi-directional DDR3/DDR3L/DDR3U/LPDDR2 I/O buffer
- Operation up to 1066MHz DDR (2133Mbps) performance with single load topology
- Designed with core and 1.8V-underdrive-1.5V IO oxide devices
- Built-in ODT (On-Die Termination)
- Flip-chip construction (area IO based)

General Description

Analog Bits' impedance programmable I/O buffer provides a high-speed physical interface solution to support the increasing bandwidths demanded by today's high-performance DDR3/DDR3L/DDR3U/LPDDR2 applications. The I/O buffer delivers up to 1066MHz/2133Mbps data rates, and serves as the integral link between the memory controller / PHY interface and the latest high-speed DDR3/DDR3L/DDR3U/LPDDR2 memory devices.

Electrical Properties

Parameter	Min	Typ	Max	Units
IO Supply Voltage VDDQ (DDR3)	1.425	1.5	1.575	V
IO Supply Voltage VDDQ (DDR3L)	1.283	1.35	1.418	V
IO Supply Voltage VDDQ (DDR3U)	1.19	1.25	1.31	V
IO Supply Voltage VDDQ (LPDDR2)	1.14	1.2	1.30	V
Core Supply Voltage VDD (core voltage options: 0.85V, 0.9V, 1.0V)	0.765 0.81 0.9	0.85 0.9 1.0	0.935 0.99 1.1	V
Temperature	-40	25	125	°C
DDR3 Performance (subject to package and topology)			1066	MHz
			2133	Mbps
DDR3L Performance (subject to package and topology)			666	MHz
			1866	Mbps
DDR3L Performance (subject to package and topology)			800	MHz
			1600	Mbps
LPDDR2 Performance (subject to package and topology)			800	MHz
			1600	Mbps

Note: All performance specifications are subject to package and topology

Deliverables and EDA Design Views

Front-end Design Views (with NDA)	Back-end Design Views (with License Agreement)
Verilog Model	GDSII stream file
Synopsys (LIB)	CDL/Spice netlist
Footprint (LEF)	Application Notes inclusive of design integration guidelines (PDF)
Datasheet (PDF)	

